1. Write C code that will enable an interrupt to be generated when the USART receives a character in asynchronous mode.

```c
IPEN = 0;  //disable priorities
RCIE = 1;  //enable RCIF interrupt
PEIE = 1;  // peripheral interrupt enable
GIE = 1;  //global interrupt enable
```

2. Draw the waveform for the byte 0xD2 sent in 8-bit, 1 start, 1 stop bit format as seen from the PIC TX pin using asynchronous communication.

```
1 (mark) 0xD2 = 0b11010010 sent as 8 data bits + 1 stop bit
0 (space)
  start bit 0 1 0 0 1 0 1 1 stop bit
  MSb
  LSb
```

3. Discuss the sequence of events that occur when an enabled interrupt is generated on the PIC18.

- The current instruction is finished.
- The return address is saved on the return address stack.
- BSR, W, Status saved in shadow registers.
- The GIE bit is set to ‘0’, disabling further interrupts.
- The PIC jumps to the interrupt vector (either high or low priority, depending on the type of interrupt), where it executes the ISR code.

4. What causes the FERR bit (framing error) to be set on asynchronous receive?

- The FERR bit is set when the stop bit is read as a ‘0’ instead of a ‘1’. This most commonly occurs if the sending baud rate is lower than the receiving baud rate.