1. Chapter 2: Problems 2.2 (hint: write an equation for $I_{ds1}$ (left schematic), then write two equations for $I_{ds2}$ – one for the top transistor (careful!!), and one for the bottom transistor. Set these two equations equal to each other because the current in these two transistors are equal. Manipulate both sides of the equation until one side looks like the $I_{ds1}$ equation and you will find that the other side is equal to one of your original $I_{ds2}$ equations, thus proving that the $I_{ds}$ current in both circuits are equal). When writing the $I_{ds}$ equations, use the linear model.

2. 2.21c, 2.21d, 2.22a,b,c,d

Answer the following short answer questions:

a. If the gate oxide (thin-ox) increases, the threshold voltage increases/decreases.

b. If the $W$ (width) of a transistor increases, the maximum current increases/decreases.

c. If the $L$ (length) of a transistor increases, the maximum current increases/decreases.

d. If a PMOS and NMOS transistors have the same $W$, $L$ values, and are each operating in saturation at a given $V_{gs}$/$V_{ds}$ point, which will produce the higher current? Explain why.

e. Give two factors that cause ‘short-channel’ devices to deviate from the ideal Shockley equations. What is the effect on drain current?

f. Using the NMOS curves in Figure 2.7 in Chapter 2, compute $V_{dsat}$ for two of the $V_{gs}$ operating points.
g. Using the curves in Figure 2.7, draw two DC power supply connections to an NFET and give the values of these two supplies such that device is operating in the linear region.

3. Assume that a 1X inverter is sized with PMOS to NMOS ratio of 2 to 1, with the unit NMOS transistor being $4\lambda/2\lambda \text{ (W/L)}$.

a. Size the transistors below to give equal pullup/pulldown current strength. Mark the transistor sizes as their ratio to an NMOS unit transistor.

b. Give the width/length of the transistors in part a in terms of lambda.

c. Assuming lambda = 90 nm, give the absolute W/L of the transistors.

d. Assume that the channel resistance $R$ is $2 \text{ k}\Omega\mu\text{m}$ (this is amount of channel resistance for NMOS transistor that is 1 \mu m wide and with minimum gate length – to get the actual resistance, divide by the actual gate width.