1. Problem 4.4

2. For the gate below, assume the NMOS transistors are sized with width = 3, and the PMOS with width = 2.
   
a. Find the Elmore delay for the worst case rise time if the load is a 4X inverter (the inverter is sized with PMOS = 2, NMOS = 1).
   b. Find the Elmore delay for the best case rise time (the ‘contamination’ delay) if the load is a 4X inverter. (the inverter is sized with PMOS = 2, NMOS = 1).