1. Design a Domino logic gate to compute \( F = (A+B)(C+D) \). Use a footer evaluation transistor, and a single precharge transistor.

2. In your design for problem #1, indicate where charge sharing may be a problem and add a secondary precharge transistor to eliminate this problem.

3. Modify the design of problem #1 to be a dual-rail domino gate.

4. Design a pseudo-NMOS gate to compute \( F = (A+B)(C+D) \).

5. Refer to the figure below, which is a 1-bit register using an edge-triggered register. Assume the DFF setup/hold times are \( T_{su} \), \( T_{thd} \) and that delay through the mux is \( T_{muxpd} \). Compute the \( T_{su} / T_{thd} \) times for the DIN input in terms of \( T_{su} \), \( T_{thd} \), and \( T_{muxpd} \). Which timing constraint, \( T_{su} \) or \( T_{thd} \), is made worse by the mux delay?

6. Problem 7.1 a, b

7. Problem 7.3, a,c

8. Problem 7.8