ECE 4263  Homework – Second homework on delay estimation

Down the associated spreadsheet, and fill in all of the BLUE cells with calculations, using the hints in comments of the YELLOW cells.

The spreadsheet provides 2D lookup tables based on output slope, input transition time for a 1X inverter and a 1X Nand2 gate.

Compute delay from P to Q

1) Compute load at N (N_load)
2) For G1, look up delay N_TPHL using P_tran, N_load and the G1 TPHL delay table.
3) For G1, look up output transition N_tran using P_tran, N_load and the G1 TPHL transition table.
4) Compute load at Q (Q_load)
5) For G2, look up delay Q_TPLH using N_tran, Q_load and the G2 a2y_TPLH delay table.
6) Delay from P to Q = G1 TPHL + G2 TPLH

Compute the path delay from P to Q for the two cases of P input rising, input falling.

Assume the pin capacitance of a 3X Nand gate is 3 * pin capacitance of 1X Nand gate, etc.

For table interpolation, round the input transition time to the next highest input transition time in the table, then do linear interpolation across the loads.

The 2D tables in the spreadsheet has output load across the top of the table, and input transition down the left hand side.

Linear interpolation for xi given points x1, F(x1), x2, F(x2) where F(x) is the table value and x is the Cap load value, with x1 < xi < x2, is:

\[ F(xi) = \frac{(F(x2) - F(x1))}{(x2 - x1)} \times (xi - x1) + F(x1) \]