1. I have a 4096 x 16 SRAM.
   a. How many address pins does it have?
   b. If the bits are arranged in square fashion in the layout (only one plane, row decoder to one side of the layout), how many rows and how many columns does the array contain?
   c. Assuming the row address is the higher order address bits, which address pins go to the row decoder, and which address pins to the column decoder?
   d. Assuming our standard 1X inverter (PMOS to NMOS width ratio is 2), how many 1X inverter loads are on the word line just counting the gate capacitance if each Wordline access transistor has a width of 2?
   e. How does the design change in (b) if I use two arrays, with the row decoder in the middle of the two arrays?

2. The IO pads we discussed in class had clamp diodes for overshoot ESD protection. How would you make a diode given the components that you have available to you in Electric? What would the geometry of that component look like?