The test is closed book/closed notes.

Gate Design
a. Be able to design a **domino logic gate** of an arbitrary non-inverting logic function.
b. Be able to design a **dual-rail domino logic** gate of an arbitrary logic function.
c. Be able to design a **psuedo-NMOS** logic gate of an arbitrary logic function.
d. Be able to size a **pseudo-NMOS pullup** if you know the resistance per micron of gate width for the pulldown and resistance per micron of gate length for the pullup to meet a VOL target.
e. Know the definition of **charge sharing** as it relates to domino logic gate design.
f. Discuss the purpose of a static keeper in a domino gate design.
g. Be able to compare and contrast **psuedo-NMOS, domino logic, and static CMOS** gate design in terms of **speed** and **power**.
h.

Sequential Logic Design
i. Be able to identify **latch, flip-flop** functionality from transistor/gate level schematics (including both **asynchronous, synchronous set/reset**).
j. Be able to discuss system timing analysis on minimum clock period for a DFF-based system, and shortest path analysis for hold-time violation checking.
k. Be able to discuss **clock skew** and its effect on setup/hold time in a DFF-based system.
l. Be able to derive **setup, hold, and clock-to-out** delay equations from transistor/gate level schematics for latches and flip-flops.

SRAMs, IO
m. Be able to design the **row, column decoding logic** for a **K x N SRAM** using a single square array.
n. Be able to draw the schematic of a **six-transistor SRAM cell**.
o. Be able to draw the schematic of an **SRAM cell with multiple read/write ports**.
p. Be able to draw the basic schematic of an **input, output, or IO pad with ESD protection**.
q. Be able to draw the transistor of a DRAM cell, and contrast DRAM against SRAM in terms of speed, density and use within a computer system.
r. Discuss the basic floating gate mechanism for non-volatile memory.
s. Be able to discuss the role of a **thick-oxide transistor** in ESD protection.
t. Be able to discuss the role of **clamping diodes** in ESD protection.

Labs:
u. Be able to discuss **standard cell** routing styles and cell design.
v. Be able to discuss the roles of **LEF, DEF, Synopsys LIB, Verilog RTL, Verilog gate-level** netlist files in a **standard cell design flow**.
w. Be able to compare contrast **standard cell** layout, **datapath** layout, and **array layout** styles in terms of their typical usage in a digital system (i.e., which layout styles would be used for what portions of the design?).